AMENDMENTS

IN THE CLAIMS

Please amend the claims as follows.

A1

1. A method of filling gaps in [the] a plane of and between [the] a pattern of interconnect lines forming a wiring structure on a semiconductor substrate, said interconnect lines having a top surface further having sidewalls, comprising the steps of:

providing a semiconductor substrate said substrate having a surface;

creating a network of interconnect lines on said surface of said substrate whereby said interconnect lines are separated by holes having bottoms between said interconnect lines thereby leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines;

[Depositing] depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including [the] said exposed surface of said semiconductor substrate;

[Performing] performing an etch back of said first layer of dielectric;

[Depositing] depositing a second layer of dielectric having a surface over said etched back first layer of dielectric;

[Etching] etching said second layer of dielectric thereby creating exposed portions of said first layer of dielectric; and

[Depositing] depositing a layer of oxide over said etched second layer of dielectric thereby including said exposed portions of said first layer of dielectric.

A1 Cont

2. The method of claim 1 wherein said interconnect lines contain [wiring structure contains] polysilicon.

3. The method of claim 1 wherein said interconnect lines contain [wiring structure contains] a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said wiring structure to be applied during the SAC process.

4. The method of claim 1 wherein said interconnect lines contain [wiring structure contains] an electrically conducting material.

A2

6. The method of claim 1 wherein said etch back of said first layer of dielectric is performing an etch back that is a Buffered Oxide based Etch said etch back to be performed on said first layer of dielectric thereby forming a layer of first

dielectric having a surface on the bottom of the holes that separate [within] said interconnect lines [wiring structure] thereby further forming deposits of said first dielectric said deposits partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby creating exposed top corners of said interconnect lines said top corners being located at intersects between said sidewalls of said interconnect lines and said top surface of said interconnect lines.

A2 cont

8. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of silicon nitride (Si_3N_4) said deposition covering the surface of said layer of first dielectric on the bottom of said holes [within] between said interconnect lines [wiring structure] thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby furthermore covering the surface of [the] said exposed top corners of said interconnect lines [wiring structure].

A3

9. The method of claim 1 wherein said depositing said second layer of dielectric is depositing a layer of Si_3N_4 using PE-CVD technology at a temperature of about 400 degrees C. whereby said

layer of Si_3N_4 is [to be] deposited to a thickness between about 1000 and 2000 Angstrom.

10. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of aluminum oxide (Al_3O_3) said deposition covering the surface of said layer of first dielectric on the bottom of said holes separating [within] said interconnect lines [wiring structure] thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby furthermore covering the surface of the partially exposed top corners of said interconnect lines [wiring structure].

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11. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material [having a high dielectric constant] said deposition covering the surface of said layer of first dielectric on the bottom of the holes separating [within] said interconnect lines [wiring structure] thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby furthermore covering surface of the partially exposed top corners of said interconnect lines [wiring structure].

12. The method of claim 1 wherein said etching said second layer of dielectric removing said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on [the] said sidewalls of said interconnect lines [wiring structure].

A3 cont

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14. The method of claim 1 wherein said depositing a layer of oxide is depositing a layer of PE-oxide or PE-TEOS (Plasma Enhanced tetraethosiloxane) over said spacers on said sidewalls of said interconnect lines [wiring structure] thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes between [within] said interconnect lines [wiring structure] thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said interconnect lines [wiring structure].

A4

15. The method of claim 1 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said

planarization to proceed down to the plane of the top surface of said conducting line pattern thereby completing the process of creating a high-aspect ratio pattern of conducting lines said conducting lines being separated with [a high dielectric constant] an Intra-Layer Dielectric.

16. A method of filling gaps in the plane of and between [the] a pattern of [a] interconnect lines forming a wiring structure on a semiconductor substrate, said interconnect lines having a top surface further having sidewalls, comprising the steps of:

A4 Cont

providing a semiconductor substrate said substrate having a surface;

creating a network of interconnect lines on said surface of said substrate whereby said interconnect lines are separated by holes having bottoms between said interconnect lines thereby leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines;

[Depositing] depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including [the] said exposed surface of said semiconductor substrate;

[Performing] performing an etch back of said a first layer of dielectric wherein said etch back is performing a Buffered Oxide Etch thereby forming a layer of first dielectric on the bottom of said holes [within] between said interconnect lines [wiring structure] thereby further forming deposits of said first dielectric on the top surfaces of interconnect lines [wiring structure] said deposits partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby creating exposed top corners of said interconnect lines said top corners being located at intersects between said sidewalls of said interconnect lines and said top surface of said interconnect lines;

A4 Cont

[Depositing] depositing a second layer of dielectric said deposition covering said layer of first dielectric on the bottom of said holes between [within] said interconnect lines [wiring structure] thereby further covering said first dielectric partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby furthermore covering the partially exposed top corners of said interconnect lines [wiring structure];

[Etching] etching said second layer of dielectric to remove said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on the sidewalls of said interconnect lines [wiring structure];

[Depositing] depositing a layer of PE-oxide or PE-TEOS over said spacers on the sidewalls of said interconnect lines [wiring structure] thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes between [within] said interconnect lines [wiring structure] thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said interconnect lines [wiring structure] thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said interconnect lines [wiring structure].

17. The method of claim 16 wherein said interconnect lines contain [wiring structure contains] polysilicon.

AP cont

18. The method of claim 16 wherein said interconnect lines contain [wiring structure contains] a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said interconnect lines [wiring structure] to be applied during the SAC process.

19. The method of claim 16 wherein said interconnect lines contain [wiring structure contains] an electrically conducting material.

22. The method of claim 16 wherein said depositing said second layer of dielectric is depositing a layer of Si_3N_4 using PE-CVD technology at a temperature of about 440 degrees C. whereby said layer of Si_3N_4 is [to be] deposited to a thickness between about 1000 and 2000 Angstrom

24. The method of claim 16 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material [having a high dielectric constant].

26. The method of claim 16 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said planarization to proceed down to the plane of the top surface of said conducting line pattern thereby completing the process of creating a high-aspect ratio pattern of conducting lines said conducting lines being separated with [a] an [high dielectric constant] Intra-Layer Dielectric.